GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES

REVIEW OF LOW POWER DUAL MODE MLMAP DECODER FOR TURBO DECODING IN VLSI TECHNOLOGY

Deepthy Bhagavathy S.K[*1], Maniraj Kumar P[2] and Sundarajan P.N[3]
PSNA college of Engineering and Technology, PG Scholar, Department of Electronics and Communication Engineering, Dindigul -624622, India[*1]
Assistant Professor, Department of Electronics and Communication Engineering, PSNA college of Engineering and Technology, Dindigul -624622, India[2,3]

ABSTRACT

In information theory, the turbo codes have received tremendous attention and have commenced their practical application due to their excellent error correcting capability. Max Log Maximum a posterior probability (MLMAP) algorithm has been widely used in turbo decoding for its outstanding performance. The MLMAP decoder examines an entire received sequence of given length. The decoder computes a metric for each path. This project presents a configurable soft MLMAP decoder implementation that meets the requirements for WLAN and broadband applications. ModelSim Simulator tool will be used for functional simulation of the design. A test bench is written in the VHDL which applies the coded data to the design of MLMAP decoding. Xilinx ISE tool will be used for FPGA synthesis.

Keywords- MLMAP decoder, turbo codes.

I. INRODUCTION

In recent years, the power consumption has become a major criteria for the use of appliances. Mainly in VLSI technology, the aim of reducing the power consumption of each decoder is in progress. Here the turbo codes with the MAP decoder are to be used as the goal to reduce power consumption. By calculating the value of some metrics, the reduction in power can be maintained. Here various approaches have been followed to reduce the power consumed but still it needs to be reduced. By the reduction of the power consumption in the decoders, the numbers of gates get reduced so that the area gets reduced and speed gets increased.

Our aim is to reduce the power consumed by the decoder circuit. This survey covers the different techniques used so for to reduce the power consumption.

II. LITERATURE SURVEY

A.Worm and H.Michel [1], focused on data transfer optimizations. The number of data transfers was a function of system level parameters, algorithmic transformations and implementation parameters. The data transfer related power consumption of turbo decoders has been significantly reduced by proper design choices. The algorithmic transformations like windowing and some control/data flow transformations were discussed. The power consumption has been minimized by the rearrangement of memory accesses.

An-Yeu (Andy) Wu and Tsung-Han Tsai [2], focused on the reduction of power consumption of the state metrics cache (SMC), low-power memory-reduced trace back maximum a posteriori algorithm(MAP) decoding was proposed. Instead of storing all state metrics, the traceback MAP decoding reduces the size of the SMC by accessing difference metrics. The proposed traceback computation requires no complicated reversion checker, path selection, and reversion flag cache. For double-binary (DB) MAP decoding, radix-2 2 and radix-4 traceback structures are introduced to provide a tradeoff between power consumption and operating frequency. These two traceback structures achieve an around 20% power reduction of the SMC, and around 7% power reduction of the DB MAP decoders. In addition, a high-throughput 12-mode WiMAX CTC decoder applying the proposed radix-2 2 traceback structure was implemented by using a 0.13- m CMOS process in a core area of 7.16 mm. Based on postlayout simulation results, the proposed decoder achieved a maximum throughput rate of 115.4 Mbps and an energy efficiency of 0.43 nJ/bit per iteration.

Dong-Soo Lee and In-Cheol Park [3], discussed that the turbo decoding was classified as a memory-intensive algorithm, reducing memory accesses is crucial to achieve a low power design. To reduce the number of memory accesses for maximum a posteriori(MAP) decoding, this paper proposed an approximate reverse calculation method that can be implemented with simple arithmetic operations such as addition and comparison. A prototype log-MAP decoder based on the proposed reverse calculation achieved 29% power reduction . This paper has presented an approximate reverse calculationto reduce the number of backward metric memory accesses required in turbo decoding. This paper has proposed a new approximation that can be implemented with simple arithmetic operations and small look-up tables, and applied the proposed reverse calculation to the backward metric processing.

Sri Parameswaran and Jörg Henkel [4], focused, fast constructive technique that relocates the instruction code in into the main memory that the cache is utilized more efficiently. The technique was applied as a preprocessing step, that is before the code is executed. The technique does not impose any computational overhead to the system. Thus, the energy consumption of the whole system (CPU, caches, buses, main memory) is reduced by upto 65%. In this paper a methodology which places instruction code in a constructive way into the

memory such that the subsequent mapping to the instruction cache leads to a reduced cache miss ratio and thus to a power/energy minimization of the whole system combined with a performance increase.

S. M. Karim and Indrajit Chakrabarti [5], focused on the performance enhancing techniques such as parallel processing and pipelining have been applied to realize the highly recursive and complex maximum a posteriori probability (MAP) decoder. The designed decoder, which achieves a throughput of 930 Mbps while consuming 265 mW of power. The proposed parallel turbo decoder has been able to achieve a BER performance within 0.03 dB of that of the serial sliding window log-MAP turbo decoder. The presented design also incorporated a collision-free interleaver that enabled parallel decoding operations. The latency of the parallel design of turbo decoder has also been drastically reduced compared to the sliding window turbo decoder. It has accomplished a throughput up to 930 Mbps while consuming silicon area of 5 mm2 and power of 265 mW in 90nm CMOS process for the turbo decoder core.

B. Bougard and L. Van Der Perre [6], analyzed the Maximum A Posteriori algorithm, the key-building block of the decoder. Therefore, it systematically optimized the data transfer and storage. This paper presented the main results of this optimization, especially those concerning the memory organization and architecture. Both for the input and the metrics values, a memory sub-layer is introduced such that temporal data locality was maximally exploited. The architecture was defined to optimally allocate memory units and assign arrays, such that the number of accesses could be drastically reduced. The combined optimizations reduce the latency by a factor 600 and the energy per bit by a factor 20, breaking definitely an important obstruction to the application of turbo codes in high-speed communication systems.It should be stressed that after memory optimization, the contribution of the data path and control logic to the total power consumption raises from 2% to 40%.This proved that the data path optimization in term of word length and normalization scheme becomes more relevant.

Jinjin He and Huaping Liu [7], presented high-speed and low-power design of Viterbi decoders for trellis coded modulation (TCM) systems.In this a pre-computation architecture incorporated with -algorithm for VD, which can effectively reduce the power consumption without degrading the decoding speed much is proposed. A general solution to derive the optimal pre-computation steps is also given in the paper. Implementation result of a VD for a rate-3/4 convolutional code used in a TCM system . The precomputation architecture reduced the power consumption by as much as 70% without performance loss, while the degradation in clock speed is negligible. In this the ACSU and SMU are modified to correctly decode the signal. The precomputation VD could reduce the power consumption by 70% with only 11% reduction of the maximum decoding speed.

Dr.S.Sutha and P.Maniraj kumar [8], proposed a scalable Maximum A-Posteriori Algorithm(MAP) processor design which can support both single-binary (SB) and double-binary(DB) decoding for high throughput decoding. The Pipelined metric architecture is proposed along with the sliding window (SW) approach in order to increase the speed of the computation. The memory requirement for storing the branch and state metrics can be reduced 45% to 55%, and synthesis result shows that the overall memory area can be reduced by 29% to 32 %, when compared to state-of-art MAP decoders. Decoder throughput of the proposed method is maintained without degrading the BER performance. The final implementation costs 122 K gate counts with XCS3S500E FPGA processor and consumes 74 mw of power consumption.

III. CONCLUSION

Here various techniques have been studied about the low power consumption. The power can be reduced by modifying the architecture using MLMAP decoder. By reducing power, speed can be increased.

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